

WE CLAIM:

1. An integrated circuit fabricated in a semiconductor of a first conductivity type, said circuit having at the surface at least one lateral MOS transistor bordered on each side by an isolation region and below said surface by a channel stop region, comprising:

a source and a drain, each comprising at said surface two regions of the opposite conductivity type, one of said regions shallow and extending to the transistor gate, the other of said regions deeper and recessed from said gate, together defining the active area of said transistor and having a depletion region when reverse biased;

said shallow regions surrounded in part by an enhanced doping implant region of the first conductivity type;

another semiconductor region, of said first conductivity type, located in each of said enhanced doping regions, having a resistivity higher than the remainder of said semiconductor, and each extending laterally approximately from the inner border of said respective shallow region to the inner border of said respective recessed region; and

said high resistivity regions extending vertically from a depth just below the depletion regions of said source and drain to approximately the top of said channel stop region.

2. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is a semiconductor epitaxial layer.

3. The circuit according to Claim 1 wherein said semiconductor material is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

4. The circuit according to Claim 1 wherein said regions of higher resistivity within said semiconductor of the first conductivity type have a resistivity at least an order of magnitude higher than the resistivity of said semiconductor of the first conductivity type.

5. The circuit according to Claim 1 wherein said depletion regions have a depth of about 40 to 50 nm from said surface so that said high resistivity regions extend vertically from about 50 to 150 nm from said surface.

6. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is made of p-type silicon in the resistivity range from about 1 to 50 Ωcm , and said source, drain, and their extensions are made of n-type silicon.

7. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of boron, aluminum, gallium, and indium, while said source, drain, their extensions, and said region of higher resistivity within said semiconductor of the first conductivity type have a dopant species selected from a group consisting of arsenic, phosphorus, antimony, and bismuth.

8. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type is made of n-type silicon in the resistivity range from about 1 to

50 Ωcm , and said source, drain, and their extensions are made of p-type silicon.

9. The circuit according to Claim 1 wherein said semiconductor of the first conductivity type has a dopant species selected from a group consisting of arsenic, phosphorus, antimony, bismuth, and lithium, while said source, drain, their extensions, and said regions of higher resistivity within said semiconductor of the first conductivity type have a dopant species selected from a group consisting of boron, aluminum, gallium, indium, and lithium.

10. The circuit according to Claim 1 wherein said gate has a narrow dimension smaller than about 0.2 μm .

11. The circuit according to Claim 1 wherein said regions of higher resistivity enhance the gain of the lateral bipolar transistor and thus the ESD protection of said MOS transistor, especially the current needed for initiating thermal breakdown, without decreasing latch-up robustness or increasing inadvertent substrate current-induced body biasing of neighboring transistors.

12. A method of increasing the p-type semiconductor resistivity in selected regions under the active area of a NMOS transistor, said regions stretching laterally between the inner borders of the extended and recessed regions of source and drain, respectively, and vertically from a depth just below the depletion regions of said source and drain to approximately the top of the channel stop region, comprising the steps of:

depositing a photoresist layer over said transistor and opening a window in said layer over said

active area of said transistor; and
implanting, at high energy, compensating n-doping
ions into said p-type semiconductor through said
window, creating deep regions having a net p-type
5 doping lower than that of said p-type
semiconductor remote from said transistor active
area.

13. A method of fabricating an NMOS transistor in the
surface of an integrated circuit, said transistor
10 having increased substrate resistance in selected p-
type semiconductor regions of said integrated circuit,
comprising the steps of:

forming non-conductive electrical isolation regions
into said p-type semiconductor for defining the
15 lateral boundaries of the NMOS transistor active
area;

depositing a first photomask layer and opening a
window therein, exposing the surface of said area
between said isolation regions;

20 implanting low-energy p-doping ions into said
exposed surface area, creating a shallow layer
suitable for adjusting the threshold voltage;

implanting high-energy p-doping ions into said
exposed surface area, creating the p-well;

25 implanting medium-energy p-doping ions into said
exposed surface area, creating a deep layer
suitable as channel stop;

removing said first photoresist layer;

growing over said surface an insulating layer, such
30 as silicon dioxide, suitable as gate dielectric,
covering said transistor area;

depositing a layer of poly-silicon or other

conductive material onto said insulating layer;
protecting a portion of said poly-silicon and
etching the remainder thereof, defining the gate
area of said transistor;
5 depositing a second photoresist layer and opening a
window therein, exposing the surface of said area
between said isolation regions;
implanting, at low energy, n-doping ions into said
exposed surface area, creating shallow n-doped
10 layers under said surface, suitable as extended
source and drain of said transistor;
implanting p-doping ions around said extended source
and drain to form pockets of enhanced p-doping
around said extended source and drain;
15 implanting high-energy compensating n-doping ions
into said exposed surface area, creating a region
at predetermined depth under said surface having
a net p-type doping lower than that of said p-
type semiconductor remote from said transistor
20 active area;
removing said second photoresist layer;
depositing conformal insulating layers of an
insulator, such as silicon nitride or silicon
dioxide, over said surface and directional plasma
25 etching said insulating layers so that only side
walls around the poly-silicon gate remain;
depositing a third photoresist layer and opening a
window therein, exposing the surface of said area
between said isolation regions;
30 implanting, at medium energy, n-doping ions into
said exposed surface area, creating an n-doped
region that extends to a medium depth under said

surface, suitable as deep source and drain of
said transistor; and

removing said third photoresist layer.

14. The method according to Claim 13 further comprising the
5 step of annealing said high energy implant at elevated
temperature.
15. The method according to Claim 13 wherein said p-type
semiconductor has a peak doping concentration between
 $4 \cdot 10^{17}$ and $1 \cdot 10^{18} \text{ cm}^{-3}$.
- 10 16. The method according to Claim 13 wherein said
implanting of low energy ions comprises ions having an
energy suitable for creating the junction at a depth
between 10 and 50 nm, and a peak concentration from
about $5 \cdot 10^{17}$ to $5 \cdot 10^{20} \text{ cm}^{-3}$.
- 15 17. The method according to Claim 13 wherein said
implanting of medium energy ions comprises ions having
an energy suitable for creating the junction at a depth
between 50 and 200 nm, and a peak concentration from
about $5 \cdot 10^{19}$ to $5 \cdot 10^{20} \text{ cm}^{-3}$.
- 20 18. The method according to Claim 13 wherein said
implanting of high energy ions comprises ions,
preferably arsenic, having an energy range from about
120 to 180 keV and a dose of about $1 \cdot 10^{12}$ to $5 \cdot$
10¹² cm^{-2} to achieve a concentration from about $1 \cdot$
25 10^{17} to $6 \cdot 10^{17} \text{ cm}^{-3}$ at a depth of more than 50 nm.
19. The method according to Claim 13 wherein said net p-
type doping of low concentration comprises a peak
concentration of about 1 to $6 \text{ E}17 \text{ cm}^{-3}$ below the p-n
junctions of said transistor's deep source and drain
30 regions.
20. A method of increasing the n-type semiconductor
resistivity in selected regions under the active area

of a PMOS transistor, said regions stretching laterally between the inner borders of the extended and recessed regions of source and drain, respectively, and vertically from a depth just below the depletion regions of source and drain to approximately the top of the channel stop region, comprising the steps of:

depositing a photoresist layer over said transistor and opening a window in said layer over said active area of said transistor; and

implanting, at high energy, compensating p-doping ions into said n-type semiconductor through said window, creating deep regions having a net n-type doping lower than that of said n-type semiconductor remote from said transistor active area.

21. A method of fabricating a PMOS transistor in the surface of an integrated circuit, said transistor having increased substrate resistance in selected n-type semiconductor regions of said integrated circuit, comprising the steps of:

forming non-conductive electrical isolation regions into said n-type semiconductor for defining the lateral boundaries of the PMOS transistor active area;

depositing a first photomask layer and opening a window therein, exposing the surface of said area between said isolation regions;

implanting low-energy n-doping ions into said exposed surface area, creating a shallow layer suitable for adjusting the threshold voltage;

implanting high-energy n-doping ions into said exposed surface area, creating the n-well;

implanting medium-energy n-doping ions into said
exposed surface area, creating a deep layer
suitable as channel stop;
removing said first photoresist layer;
5 growing over said surface an insulating layer, such
as silicon dioxide, suitable as gate dielectric,
covering said transistor area;
depositing a layer of poly-silicon or other
conductive material onto said insulating layer;
10 protecting a portion of said poly-silicon and
etching the remainder thereof, defining the gate
area of said transistor;
depositing a second photoresist layer and opening a
window therein, exposing the surface of said area
15 between said isolation regions;
implanting, at low energy, p-doping ions into said
exposed surface area, creating shallow p-doped
layers under said surface, suitable as extended
source and drain of said transistor;
20 implanting n-doping ions around said extended source
and drain to form pockets of enhanced n-doping
around said extended source and drain;
implanting high-energy compensating p-doping ions
into said exposed surface area, creating a region
25 at predetermined depth under said surface having
a net n-type doping lower than that of said n-
type semiconductor remote from said transistor
active area;
removing said second photoresist layer;
30 depositing conformal insulating layers of an
insulator, such as silicon nitride or silicon
dioxide, over said surface and directional plasma

etching said insulating layers so that only side walls around the poly-silicon gate remain; depositing a third photoresist layer and opening a window therein, exposing the surface of said area between said insulation regions; implanting, at medium energy, n-doping ions into said exposed surface area, creating an p-doped region that extends to a medium depth under said surface, suitable as deep source and drain of said transistor; and removing said third photoresist layer.

22. The method according to Claim 21 wherein said n-type semiconductor has a peak doping concentration between $4 \cdot 10^{17}$ and $1 \cdot 10^{18}$ cm⁻³.
23. The method according to Claim 21 wherein said implanting of low energy ions comprises ions having an energy suitable for creating the junction at a depth between 10 and 50 nm, and a peak concentration from about $5 \cdot 10^{17}$ to $5 \cdot 10^{20}$ cm⁻³.
24. The method according to Claim 21 wherein said implanting of medium energy ions comprises ions having an energy suitable for creating the junction at a depth between 50 and 200 nm, and a peak concentration from about $5 \cdot 10^{19}$ to $5 \cdot 10^{20}$ cm⁻³.
25. The method according to Claim 21 wherein said implanting of high energy ions comprises ions, preferably arsenic or phosphorus, having an energy range from about 120 to 180 keV and a dose of about $1 \cdot 10^{12}$ to $5 \cdot 10^{12}$ cm⁻² to achieve a concentration from about $1 \cdot 10^{17}$ to $6 \cdot 10^{17}$ cm⁻³ at a depth of more than 50 nm.
26. The method according to Claim 21 wherein said net n-

type doping of low concentration comprises a peak concentration of about 1 to 6 E17 cm-3 below the p-n junctions of said transistor's deep source and drain regions.

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